8-inch wafer sensor production at Tezzaron/ Novati

February 13, 2017

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U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

8-inch Wafer Sensor Production at Tezzaron/Novati

- Effort led by **Ron Lipton of FNAL**
- Two sensor runs completed
  - 1st run completed May 2015
    - 4 float-zone wafers
    - Feasibility was confirmed
  - 2nd run completed in March 2016 with U.S. SBIR Phase 1 funding
    - 2 float-zone plus 4 SOI wafers
    - Results were promising
      - Guard ring breakdown voltages inconsistent, possibly due to unintended blanket p-type implant
- 3rd run in design, Phase 2 SBIR funding approved

8” Tezzaron/Novati Phase 2 Run

“Phase 2” funding received – Development of AC coupling/polysilicon resistors

Plan to use SOI-based process (no Si-Si)

- Bond backside implanted FZ device wafer to handle wafer
- Thin device wafer to 200 microns, polish
- After sensor processing, remove handle and backside oxide
- Process splits
  - p-stop split: 5E12 & 5E11 at 80KeV
  - n+ split: 1E16 and 1E15
  - DC only (skip polysilicon and AC cap steps) split?

Wafer design underway

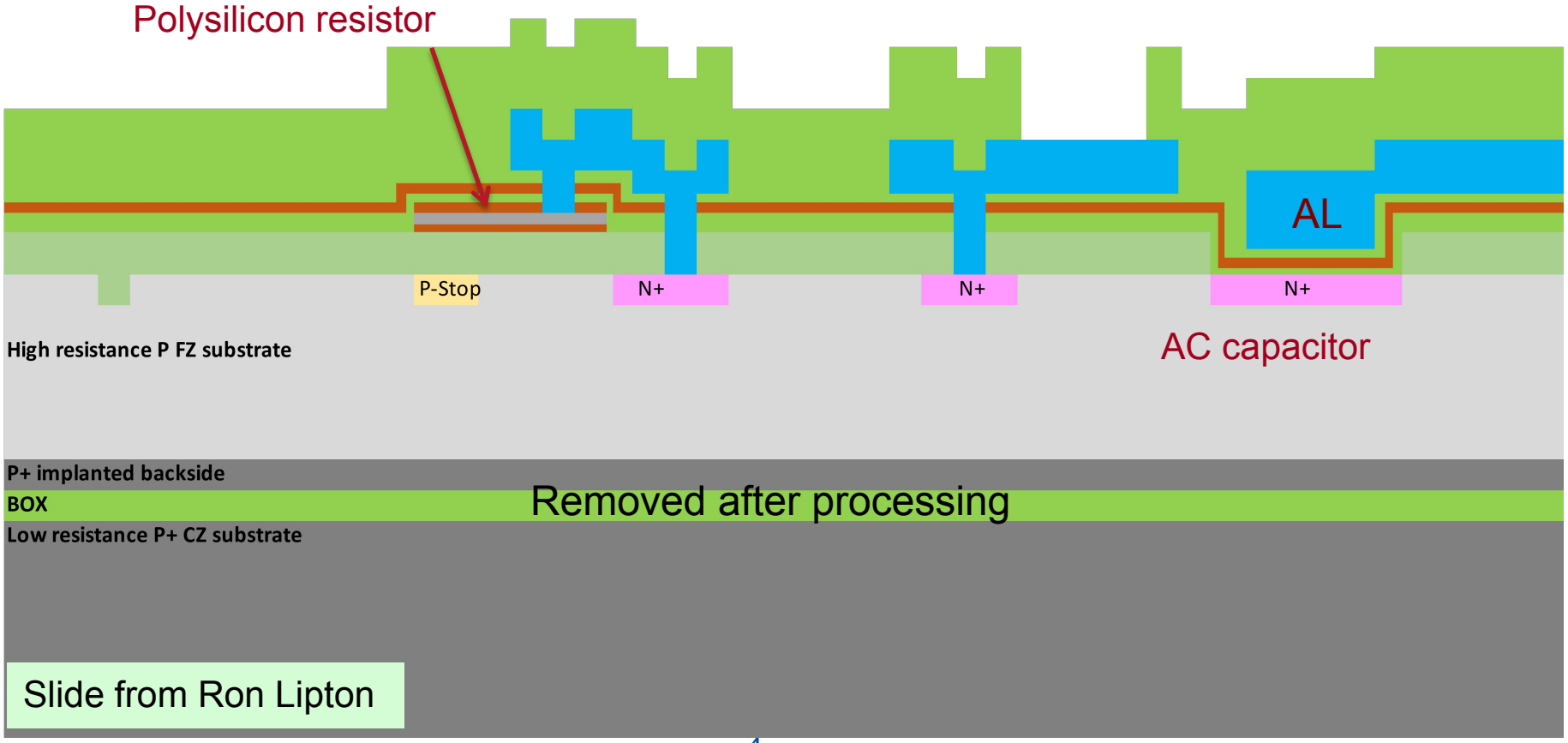
- Will include PS-s sensor to test AC and poly process
- HGC half hexagon
- Also designs from Argonne, SLAC, CMS, FCP130 pixel
- Hope to start processing in Mid April

Slide from Ron Lipton

Process Details

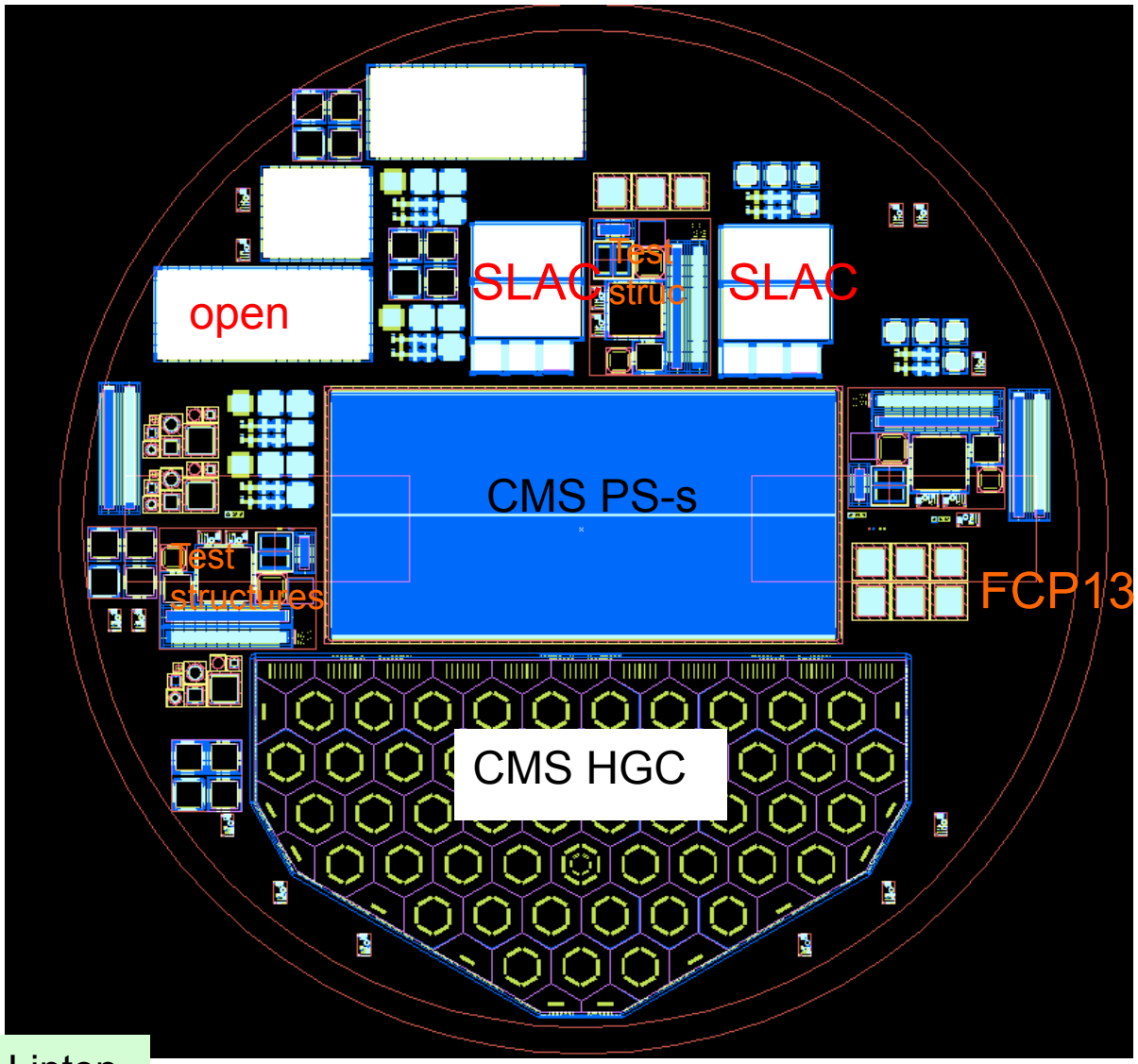
FZ device wafers are backside implanted before forming the SOI sandwich. The SOI wafer is annealed at 1200 deg.

- Can use this as a gettering step (roughen surface)
- FZ resistivity is 2k-3.5K Ohm-cm (lower than >5k Phase 1)
- Add polysilicon resistor and AC capacitor



Slide from Ron Lipton

Current Phase 2 Wafer Layout



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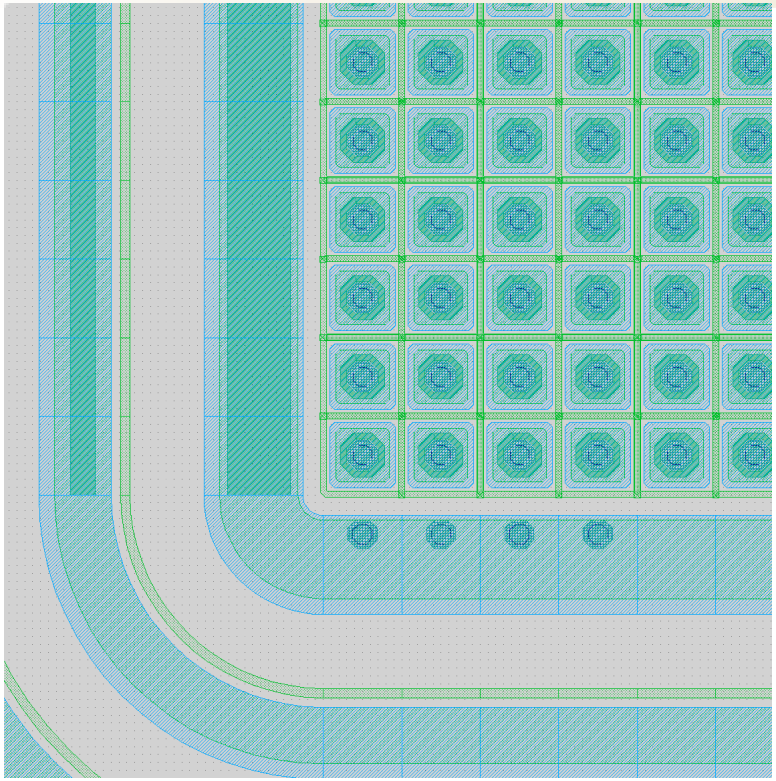
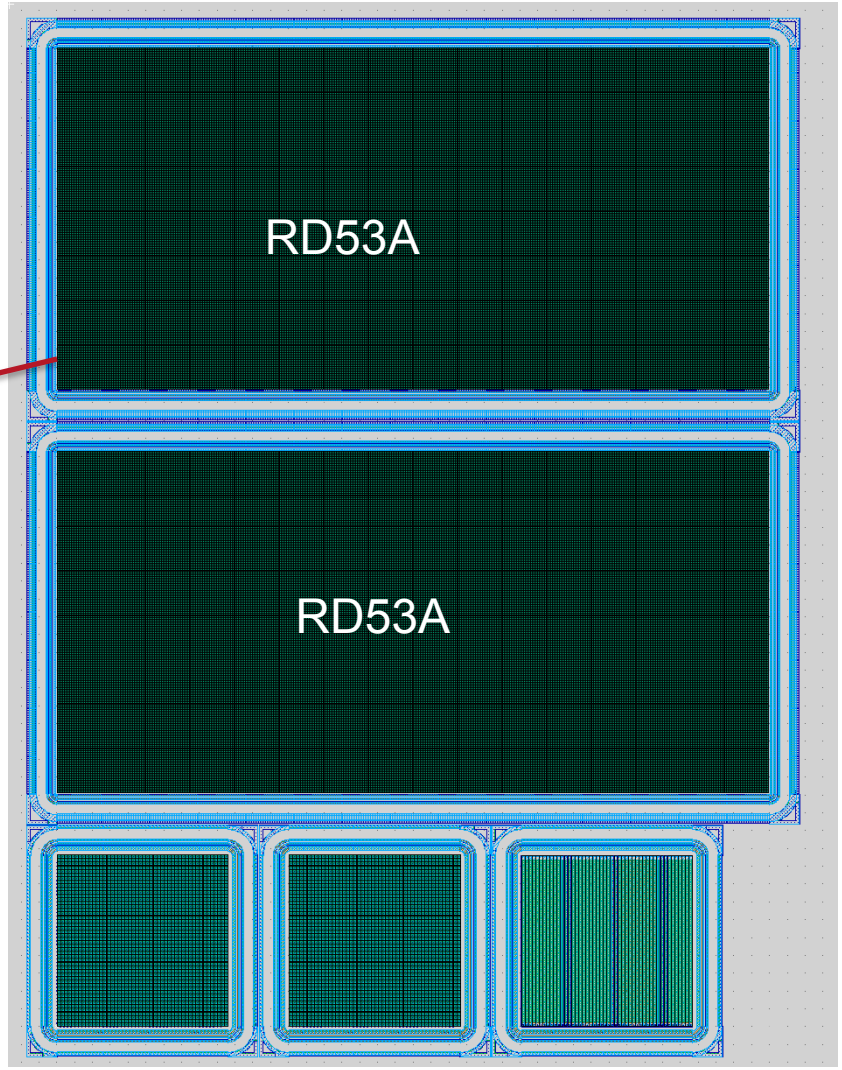
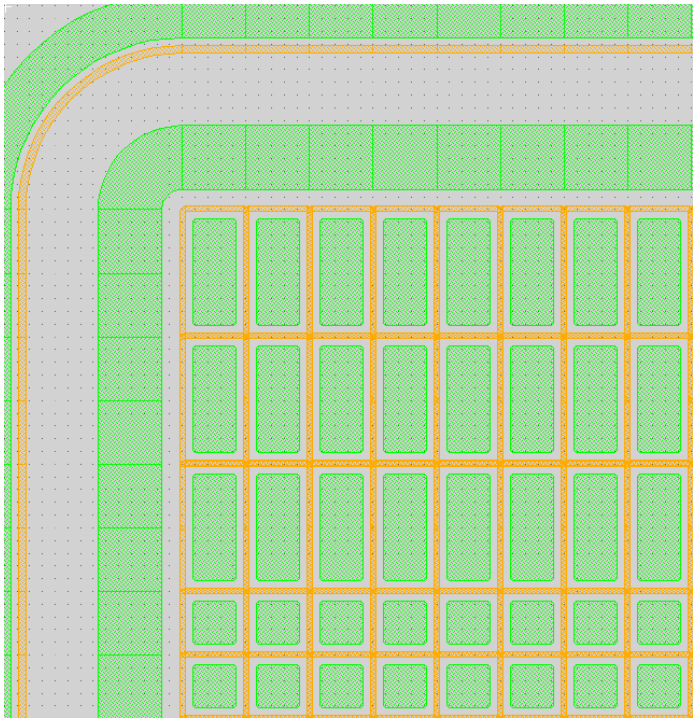
SLAC Layout for Phase 2 Run (Preliminary)

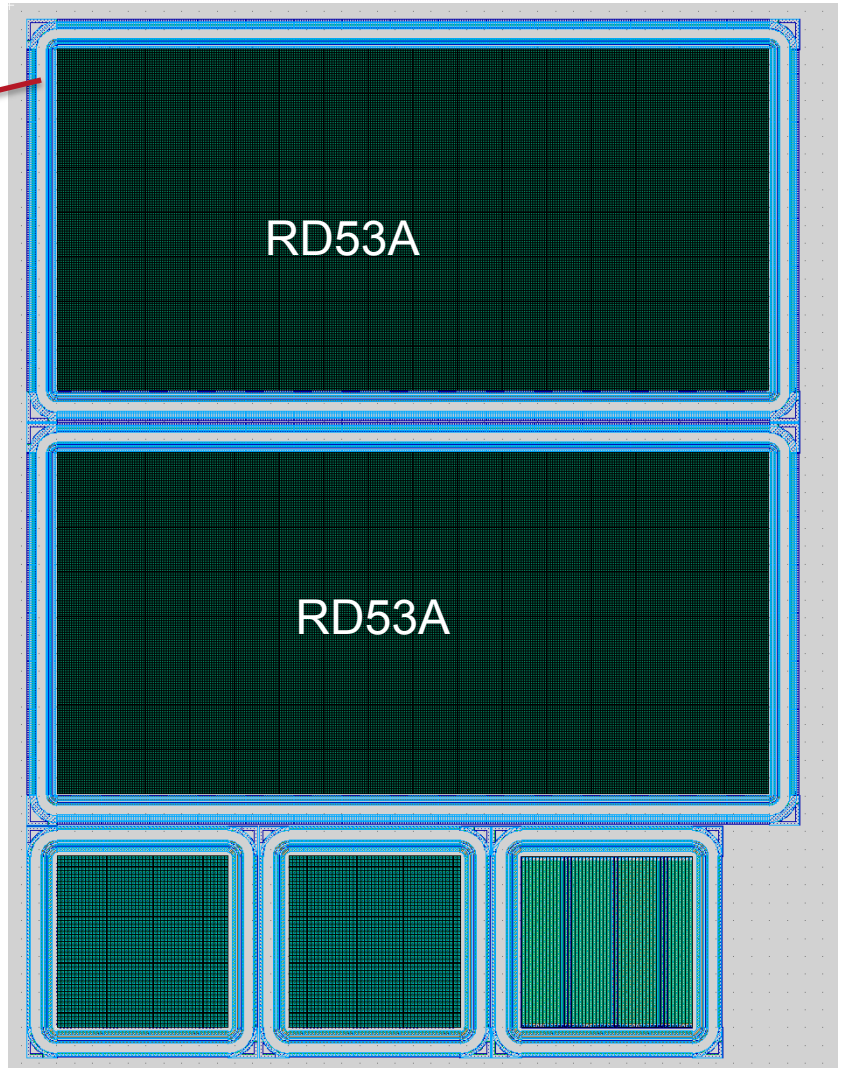




- SLAC will design two RD53A sensors
- We will co-ordinate with ETH Zurich/ Bonn effort (M. Backhaus)
  - They plan 50μm square cell and 25μm x 100μm cell RD53 versions

SLAC Layout for Phase 2 Run (Preliminary)



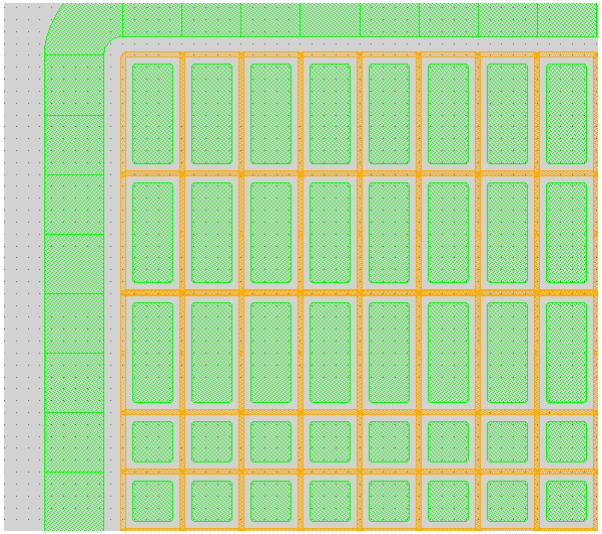


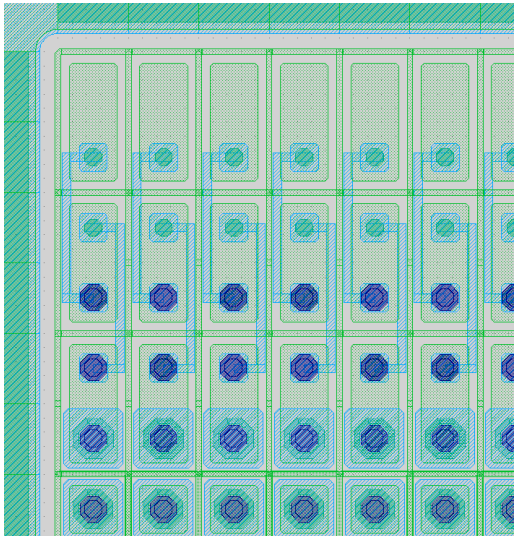
One RD53 sensor will have “stretch” cells to test concept for intra-ASIC region

SLAC Layout for Phase 2 Run (Preliminary)

Possible “stretch” layouts

3 rows of larger cells: may require metal routing that increases capacitance





2 rows of larger cells